L Number	Hits	Search Text	DB	Time stamp
1	1	("6222269").PN.	USPAT; US-PGPUB	2002/12/27 09:18
2	141	(light adj absorbing) with (via or trench)	USPAT; US-PGPUB	2002/12/27 09:19
3	27	((light adj absorbing) with (via or trench)) and dielectric	USPAT; US-PGPUB	2002/12/27 09:19

US-PAT-NO: 6406995

DOCUMENT-IDENTIFIER: US 6406995 B1

TITLE: Pattern-sensitive deposition for damascene processing

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In the embodiment where third mask layer 170 is a positive photoresist, the
photoresist is coated over dielectric layer 130. A mask or reticle is then
used to expose a portion of the photoresist to a light source. The exposed
portion defines a trench over via 150. The exposed portion includes an area
over sacrificial material 160. Because sacrificial material 160 is generally
insensitive to a photoreaction, sacrificial material 160 is not affected by the
exposure to, for example, an UV light source. Sacrificial material 160 is
insensitive either in that it does not contain any photo-active components or
has been treated, for example, by heat, to inactivate its sensitivity to a
photoreaction. Alternatively, a photoresist containing a light-absorbing dye
(e.g., a dyed photoresist) may be used as sacrificial material 160. In this
embodiment, upon light exposure to define an etch pattern for a subsequent
trench in dielectric layer 130, the **light-absorbing** dye absorbs any UV light
striking sacrificial material 160. Thus, a trench patterning step to pattern a
photoresist mask over dielectric layer 130 will not significantly effect
sacrificial material 160.

DOCUMENT-IDENTIFIER: US 20020182894 A1

TITLE: METHOD OF MAKING A SEMICONDUCTOR DEVICE USING A SILICON CARBIDE HARD
MASK

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[0022] Still another process for making a semiconductor device, which may
benefit from use of the method of the present invention, is illustrated in
FIGS. 4a-4e. In that process, **via** 407 is filled with sacrificial **light**
absorbing material ("SLAM") 408 to create the structure shown in FIG. 4a. That
SLAM may comprise a dyed spin-on-polymer ("SOP") or dyed spin-on-glass ("SOG")
that has dry etch properties similar to those of dielectric layer 403 and light
absorbing properties that enable the substrate to absorb light during
lithography. SLAM 408 may be spin coated onto the FIG. 1c structure in the
conventional manner.

US-PAT-NO: 6465358

DOCUMENT-IDENTIFIER: US 6465358 B1

TITLE: Post etch clean sequence for making a semiconductor device

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A process has been proposed to address these issues. In that process, the via
is filled with a sacrificial material prior to etching the trench. Filling the
via with that material enables the trench to be etched using an etch chemistry
that ensures high quality via and trench profiles, without having to consider
the relative selectivity between the dielectric layer and the protective layer.
That sacrificial material may be dyed or covered with an appropriate
antireflective coating to produce a **light absorbing** background that ensures
uniform reflectivity of light used to expose the photoresist during **trench**
patterning. Examples of this process are described in copending applications
Ser. Nos. 09/422,821 and 09/501,354 (filed Oct. 21, 1999 and Feb. 9, 2000,
respectively, and each assigned to this application's assignee).

US-PAT-NO: 6448185

DOCUMENT-IDENTIFIER: US 6448185 B1

TITLE: Method for making a semiconductor device that has a dual damascene
interconnect

---------- KWIC ---------

Dual damascene metal interconnects may enable reliable low cost production of
integrated circuits using sub 0.18 micron process technology. To enable such
interconnects to realize their full potential, the following method for making
a semiconductor device has been proposed. In that method, a first etched
region (e.g., a **via or trench**) is filled with a sacrificial **light absorbing**
material ("SLAM"), after that region has been formed within a dielectric layer.
That SLAM may comprise a dyed spin-on-glass ("SOG") that has dry etch
properties similar to those of the dielectric layer and light absorbing
properties that enable the substrate to absorb light during lithography. After
the first etched region is filled with the SLAM, a second etched region (e.g.,
a trench if the via is already formed or a via if the trench is already formed)
is formed within the dielectric layer. Most of the SLAM may be removed as that
second etched region is formed. Remaining portions of the SLAM are removed by
a subsequent wet etch step.

After **via** 107 is formed through dielectric layer 103, **via** 107 is filled with
sacrificial **light absorbing** material ("SLAM") 104, generating the structure
shown in FIG. 1d. SLAM 104 has dry etch properties similar

to those of
dielectric layer 103, but may be wet etched at a rate that is significantly
faster than the rate at which dielectric layer 103 may be wet etched. Such dry
etch properties should enable removal of most of SLAM 104 at the same time the
dielectric layer is etched to form the trench. The high selectivity of SLAM
104 to the wet etch enables removal of that material from the surface of the
device, as well as from inside via 107, without causing a significant amount of
dielectric layer 103 to be removed at the same time.

By filling **via** 107 with a sacrificial **light absorbing** material having dry etch
characteristics like those of CDO containing dielectric layer 103, the **trench**
lithography process effectively applies to a substantially "hole-free" surface,
similar to one without vias. By selecting an appropriate dyed SOG material for
SLAM 104, and an appropriate etch chemistry, trench 106 may be etched into
dielectric layer 103 at approximately the same rate that SLAM 104 is removed.
Because such a process protects the underlying barrier layer 102 as trench 106
is etched, it permits use of a trench etch chemistry that produces superior
trench and via profiles without having to consider its effect on the
selectivity between dielectric layer 103 and barrier layer 102. For example,
when barrier layer 102 comprises silicon nitride or silicon carbide, this
process enables use of an etch chemistry to etch the trench that does not
provide a high selectivity to CDO over silicon nitride or silicon carbide.

9. A method of forming a semiconductor device having a dual damascene
interconnect comprising: forming a first conductive layer on a substrate;
forming a barrier layer on the surface of the first

conductive layer; forming a dielectric layer that comprises a carbon doped oxide on the surface of the barrier layer; patterning a first layer of photoresist, after forming the dielectric layer, to define a via; forming a via through a first portion of the dielectric layer; filling the **via** with a sacrificial **light absorbing** layer that comprises a dyed SOG; patterning a second layer of photoresist to define a trench; forming a **trench** within the dielectric layer by removing part of the sacrificial **light absorbing** layer and a second portion of the dielectric layer; exposing the resulting device to a plasma generated from a forming gas that comprises a mixture of hydrogen and a gas selected from the group consisting of nitrogen, helium, argon, krypton, neon, and xenon, followed by exposing it to a solution that comprises hydrogen fluoride in either ethylene glycol or deionized water; and then filling the via and trench with a second conductive layer.

13. A method of forming a semiconductor device having a dual damascene interconnect comprising: forming a first conductive layer that comprises copper on a substrate; forming a barrier layer that comprises silicon nitride on the surface of the first conductive layer; forming a dielectric layer that comprises a carbon doped oxide on the surface of the barrier layer; patterning a first layer of photoresist, after forming the dielectric layer, to define a via; forming a via through a first portion of the dielectric layer; filling the **via** with a sacrificial **light absorbing** layer that comprises a dyed SOG; patterning a second layer of photoresist to define a trench; forming a **trench** within the dielectric layer by removing part of the sacrificial **light absorbing**

layer and a second portion of the dielectric layer; exposing the resulting device to a plasma generated from a forming gas that comprises a mixture of hydrogen and a gas selected from the group consisting of nitrogen, helium, argon, krypton, neon, and xenon, followed by exposing it to a solution that comprises hydrogen fluoride in either ethylene glycol or deionized water; removing a portion of the barrier layer; and then filling the via and trench with a second conductive layer that comprises copper.